restarting the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

REMARKS

In view of the amendments set forth above, it is respectfully submitted that the application is in condition for allowance and action to that effect is respectfully requested at an early date. If the Examiner feels that a telephone conference would expedite allowance of this application, the Examiner is invited to call the undersigned at (831) 655-2300.

The Commissioner is authorized to charge any additional fees that may be due to our Deposit Account No. 50-0388 (Order No. LAM1P154).

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: ANNAPRAGADA et al.

Attorney Docket No.: LAM1P154

Application No.: 09/688,021

Examiner: UNKNOWN

Filed: October 13, 2000

Group: 1765

Title: PROCESS FOR ETCHING VIAS IN ORGANOSILICATE GLASS MATERIALS WITHOUT CAUSING RIE LAG

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Assistant Commissioner for Patents, Washington, DC 20231 on March 12, 2001.

Signed: Sandra Halliwell

CLEAN VERSION OF PENDING CLAIMS (PRELIMINARY AMENDMENT)

Please replace the entire Claims section of the referenced patent application, starting on page 12, line 1, with the following:

CLAIMS

What is claimed is:

1. A method for etching a feature with minimal RIE lag in an integrated circuit wafer incorporating at least one layer of organosilicate glass dielectric, the method comprising:

positioning the wafer in a reaction chamber;

introducing a flow of etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

striking a plasma with the etchant gas in the reaction chamber.

2. The method, as recited in claim 1, wherein the etchant gas mixture further comprises CH2F2.

3. The method, as recited in claim 2, wherein the etchant gas mixture further comprises oxygen.

4. The method, as recited in claim 3, wherein the etchant gas mixture further comprises argon.

5. The method, as recited in claim 4, further comprising etching a first layer of organosilicate glass dielectric with the plasma from the etchant gas comprising C4F8, CF4, CH2F2, oxygen and argon.

6. The method, as recited in claim 5, further comprising stopping the flow of CH2F2 and C4F8 in the etchant gas and using the resulting plasma to etch through an etch stop layer.

7. A method for etching a feature with minimal RIE lag in an integrated circuit wafer, the method comprising:

positioning the wafer in a reaction chamber;

etching through a first layer of organosilicate glass dielectric, comprising:

providing a flow of an etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

8. The method, as recited in claim 7, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises CH2F2.

9. The method, as recited in claim 8, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises oxygen.

10. The method, as recited in claim 9, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises argon.

11. The method, as recited in claim 10, further comprising etching through an etch stop layer, comprising:

providing an etchant gas mixture without C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

12. The method, as recited in claim 10, further comprising etching through an etch stop layer after etching through the first layer of organosilicate glass, comprising:

stopping the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

13. The method, as recited in claim 12, further comprising etching through a second layer of organosilicate glass dielectric, comprising:

restarting the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

14. The method, as recited in claim 13, further comprising stripping a photoresist mask, comprising:

stopping the flow of C4F8 and CF4 into the reaction chamber;

providing a flow of nitrogen into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

15. An integrated circuit formed by the method comprising:

positioning a wafer in a reaction chamber;

etching through a first layer of organosilicate glass dielectric over the wafer, comprising:

providing a flow of an etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

16. The integrated circuit, as recited in claim 15, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises CH2F2, oxygen, and argon.

17. The integrated circuit, as recited in claim 16, wherein the method further comprises etching through an etch stop layer, comprising:

providing an etchant gas mixture without C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

18. The integrated circuit, as recited in claim 16, wherein the method further comprises etching through an etch stop layer after etching through the first layer of organosilicate glass, comprising:

stopping the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the resulting etchant gas in the reaction chamber.

19. The integrated circuit, as recited in claim 18, wherein the method further comprises etching through a second layer of organosilicate glass dielectric, comprising:

restarting the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

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